In the Claims:

Claims 16-24 are withdrawn.
Please cancel claims 10 and 11.
Please enter amended claims 1-8, 12-16, and 22.
Please add claims 25-33.

1. (currently amended) A method for forming a non-volatile memory embedded logic circuit comprising the steps of:

providing a semiconductor substrate;

forming an isolation ~~region~~ structure on said semiconductor substrate to ~~define~~ isolate a first ~~active~~ device area, a second ~~active~~ device area, and a third ~~active~~ device area;

forming a first oxide layer on said first, second, and third ~~active~~ device areas simultaneously, said first oxide layer providing a high voltage logic gate oxide layer in said second device area;

etching said first oxide layer in said first and ~~second active~~ third device areas to expose said substrate ~~underneath~~;

forming a second oxide layer in said first ~~active~~ device area simultaneously with said ~~and second active~~ third device area, ~~thereby~~ providing a tunnel oxide layer in said first ~~active~~ device area, a low voltage logic gate oxide layer in said ~~second active~~ third device area~~, and a high voltage logic gate oxide layer in said third active area~~; and

forming a floating gate layer on top of said first oxide layer[[s]].

2. (currently amended) The method of claim 1, wherein said isolation ~~region~~ structure is formed by a shallow trench isolation method.

3. (currently amended) The method of claim 1, wherein said isolation ~~region~~ structure is formed by a local oxidation of silicon method.

4. (currently amended) The method of claim 1, wherein said first oxide layer[[s are]] is formed by thermal oxidation.

5. (currently amended) The method of claim [[2]] 1, wherein said first oxide layer[[s are]] is formed by chemical vapor deposition.

6. (currently amended) The method of claim [[2]] 1, wherein said first oxide layer[[s are]] is formed by atomic layer deposition.

7. (currently amended) The method of claim 1, wherein said first oxide layer is formed to approximately 250 Å thick.

8. (currently amended) The method of claim 1, wherein said second oxide layer is formed to approximately 70 Å thick.

9. (original) The method of claim 1, wherein said floating gate layer is a doped polysilicon layer.

10-11 (Cancelled)

12. (currently amended) A method for forming a non-volatile memory embedded logic circuit comprising the steps of:

providing a semiconductor substrate;

forming an isolation ~~region~~ structure on said semiconductor substrate to define a first ~~active~~ device area and a second ~~active~~ device area;

forming a first oxide layer on said first and second ~~active~~ device areas simultaneously, said first oxide layer forming a high voltage logic gate oxide layer in said second device area;

etching said first oxide layer in said first ~~active~~ device area to expose said substrate ~~underneath~~;

forming a second oxide layer in said first ~~active~~ device area, ~~thereby~~ providing a tunnel oxide layer in said first ~~active~~ device area~~, and a high voltage logic gate oxide layer in said second active device area~~; and

forming a floating gate layer on top of said second oxide layers.

13. (currently amended) The method of claim [[10]] 12, wherein said first oxide layer[[s are]] is formed by thermal oxidation.

14. (currently amended) The method of claim [[10]] 12, wherein said second oxide layer is formed to approximately 70 Å thick.

15. (currently amended) The method of claim [[10]] 12, wherein said ~~conductive layer~~ floating gate layer is a doped polysilicon layer.

16-24 (withdrawn)

25. (new) The method of claim 1, wherein said second oxide layer is formed by thermal oxidation.

26. (new) The method of claim 1, wherein said second oxide layer is formed by chemical vapor deposition.

27. (new) The method of claim 1, wherein said second oxide layer is formed by atomic layer deposition.

28. (new) The method of claim 12, wherein said first oxide layer is formed by chemical vapor deposition.

29. (new) The method of claim 12, wherein said first oxide layer is formed by atomic layer deposition.

30. (new) The method of claim 12, wherein said second oxide layer is formed by thermal oxidation.

31. (new) The method of claim 12, wherein said second oxide layer is formed by chemical vapor deposition.

32. (new) The method of claim 12, wherein said second oxide layer is formed by atomic layer deposition.

33. (new) The method of claim 12, wherein said first oxide layer is approximately 250 Å thick.